In the paragraph beginning on page 10, line 22:

94 Fig. 21 shows an exemplary timing jitter sequence $\Delta\varphi[n]$.

In the paragraph beginning on page 13, line 11:

95 In the clock skew measuring method of the present embodiment, the distributed clocks to be measured are selected and brought out to the outside of the chip by means of a clock signal selector, for example, a multiplexer. Then, the time difference between the edge timing of the clock signal and the reference timing is measured for each of the selected clock signals, so that the difference between the time differences thus measured is obtained, thereby measuring the clock skew. For simplification, the method for measuring the skew between two distributed clock signals is described below.

IN THE CLAIMS:

Please amend claims 3-5, 7-8, 13-14, 20-22, 24-25, and 31 as shown below. Marked-up versions of the amended claims are attached.

96 3. A clock skew measuring apparatus as claimed in claim 1, wherein said clock skew estimator measures a deterministic component of said clock skew between said plurality of clock signals to be measured.

4. A clock skew measuring apparatus as claimed in claim 1, wherein said clock skew estimator measures a random component of said clock skew between said plurality of clock signals to be measured.

5. A clock skew measuring apparatus as claimed in claim 1, wherein said clock skew estimator includes:

a timing estimator operable to obtain a reference timing that is an edge timing of said reference signal and a tested timing that is an edge timing of each of said plurality of clock signals to be measured;